

**WHAT IS CLAIMED IS:**

1. A method of manufacturing a semiconductor device comprising the steps of:

- 5           forming an insulating layer on a silicon substrate;  
          forming a contact hole on the insulating layer;  
          forming a nitride layer on the side of the contact  
hole; and  
          forming a selective conductive plug in the contact  
10 hole, including on the nitride layer.

2. The method of manufacturing a semiconductor device according to claim 1, wherein, prior to the step of forming the insulating layer, further comprising the steps of:

- 15           forming a gate structure on the silicon substrate;  
          forming an insulating layer spacer on the gate structure; and  
          forming an oxide layer on the insulating layer spacer  
on the gate structure.

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3. The method of manufacturing a semiconductor device according to claim 2, wherein the step of forming the oxide layer comprises the steps of forming an oxide layer on the whole structure, including the insulating layer spacer, and  
25 selectively removing the oxide layer by using a wet etch

process so that only the insulating layer spacer on the gate structure remains.

4. The method of manufacturing a semiconductor device according to claim 1, wherein the selective conductive plug comprises a selective single crystal silicon grown on the surface of the silicon substrate and selective polycrystalline silicon grown on the nitride layer of the side of the contact hole.

5. The method of manufacturing a semiconductor device according to claim 4, wherein the selective conductive plug is formed in accordance with LPCVD or UHVCVD.

6. The method of manufacturing a semiconductor device according to claim 2, wherein the oxide layer includes a PE-USG oxide layer.

7. The method of manufacturing a semiconductor device according to claim 6, wherein the PE-USG oxide layer is deposited under the conditions that the flow rate of  $\text{SiH}_4$  is between 10 and 200sccm, the flowrates of  $\text{N}_2\text{O}$  and  $\text{O}_2$  are between 100 to 3000sccm, respectively, and the flowrate of He is up to 1000sccm.

8. The method of manufacturing a semiconductor device according to claim 6, wherein the PE-USG oxide layer is deposited at a pressure of between 0.1 and 100 Torr, at a temperature of between 350 and 600°C and a power of between 100 and 1000 Watts.

9. The method of manufacturing a semiconductor device according to claim 7, wherein the PE-USG oxide layer has a thickness of between 300 and 1000 Å and a step coverage below 50%.

10. The method of manufacturing a semiconductor device according to claim 2, wherein the insulating layer spacer is an oxide layer or a nitride layer.

11. The method of manufacturing a semiconductor device according to claim 3, wherein the wet etch process is performed at a temperature of between 50 and 100°C in distilled water mixed to a ratio of between 50 to 500 times by using a diluted HF solution.

12. The method of manufacturing a semiconductor device according to claim 3, wherein the wet etch process is performed under the conditions that  $H_2SO_4$  and  $H_2O_2$  solutions are maintained at the ratio of between 1:1 and 100:1 and the

temperature is between 80 and 120°C, for 1 and 20 minutes.

13. The method of manufacturing a semiconductor device according to claim 3, wherein the reactive ion etch process  
5 is additionally performed after the wet etch process.

14. The method of manufacturing a semiconductor device according to claim 10, wherein the step of forming the nitride layer is performed by forming the nitride layer on  
10 the gate structure, including over the oxide layer spacer, and then by selectively removing the nitride layer by a dry etch process.

15. The method of manufacturing a semiconductor  
15 device according to claim 14, wherein the dry etch process is performed by using  $\text{NF}_3$  and  $\text{O}_2$  gas plasma, under the conditions that the flow rate of  $\text{NH}_3$  is between 10 and 50sccm, the flowrate of  $\text{O}_2$  is between 30 and 300sccm, the flowrate of He is between 100 and 2000sccm, at a power of between 1 and  
20 200 Watts, a pressure of between 1mTorr and 10Torr, and a temperature of about 200°C.

16. The method of manufacturing a semiconductor device according to claim 2, wherein an in-situ cleaning  
25 process is performed after the contact hole is formed.

17. The method of manufacturing a semiconductor device according to claim 16, wherein the in-situ cleaning process is performed by using a H<sub>2</sub> bake, under the conditions that the flow rate of Hydrogen is between 5 and 150slm, a pressure of between 1 and 200Torr, and a temperature between 750 and 950°C, for between 5 and 30 minutes.

18. The method of manufacturing a semiconductor device according to claim 16, wherein the in-situ cleaning process and selective conductive plug formation process are performed in the same chamber.

19. The method of manufacturing a semiconductor device according to claim 16, wherein the in-situ cleaning process is performed by using a RTP under the conditions that the temperature is raised to 950°C at a ramping rate of between 10 and 100°C/sec.

20. The method of manufacturing a semiconductor device according to claim 4, wherein the selective conductive plug is formed by applying a DCS-H<sub>2</sub>-HCl gas system, under the conditions that the temperature is to 750 and 850°C, the pressure between is 5 and 150 Torr, the flow rate of DCS is between 0.1 and 1slm, the flowrate of HCl is between 0.1 and 1.0slm, and the flowrate of H<sub>2</sub> is between 30 and 150slm.

21. The method of manufacturing a semiconductor device according to claim 4, wherein the selective conductive plug is formed by applying a MS-H<sub>2</sub>-HCl gas system, under the conditions that the temperature is between 750 to 950°C, the pressure is between 5 and 150 Torr, the flow rate of MS is between 0.1 and 1slm, the flowrate of HCl is between 0.5 and 5.0 slm, and the flowrate of H<sub>2</sub> is between 30 and 150slm.

22. The method of manufacturing a semiconductor device according to claim 4, wherein the selective conductive plug is formed by applying a Si<sub>2</sub>H<sub>6</sub>+Cl<sub>2</sub>+H<sub>2</sub> gas system, under the conditions that flow rate of Si<sub>2</sub>H<sub>6</sub> is between 0.1 and 10sccm, the flowrate of Cl<sub>2</sub> is up to 5.0sccm, and the flowrate of H<sub>2</sub> is up to 20sccm.

23. The method of manufacturing a semiconductor device according to claim 4, wherein the selective conductive plug is formed in-situ by using H<sub>2</sub> gas, including 1 to 10% PH<sub>3</sub>.

24. The method of manufacturing a semiconductor device according to claim 4, wherein GeH<sub>4</sub> gas is supplied at up to 10sccm during the formation of the selective conductive plug.

25. The method of manufacturing a semiconductor device according to claim 4, wherein the selective conductive plug is deposited in UHVCVD for single wafer process and in UHVCVD for tube type SEG.

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26. The method of manufacturing a semiconductor device according to claim 16, wherein the in-situ cleaning process is performed in a LPCVD chamber or a UHVCVD chamber.

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27. The method of manufacturing a semiconductor device according to claim 1, further comprising the step of performing a plasma treatment on the silicon substrate having the nitride layer.

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28. The method of manufacturing a semiconductor device according to claim 27, wherein the plasma treatment is performed by using a  $\text{NF}_3 + \text{O}_2$  processing gas, under the conditions that the flowrate of  $\text{NH}_3$  is between 10 and 100sccm, the flowrate of  $\text{O}_2$  is between 30 and 300sccm, the flowrate of He is between 100 and 2000sccm, at a power of between 1 and 200 Watts, a pressure of between 1mTorr and 10Torr, and a temperature of about 200°C.

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29. The method of manufacturing a semiconductor device according to claim 27, wherein the selective conductive plug comprises a selective single crystal silicon grown on the surface of the silicon substrate and selective  
5 polycrystalline silicon grown on the nitride layer on contact hole side.

30. The method of manufacturing a semiconductor device according to claim 27, wherein the selective  
10 conductive plug is formed in accordance with LPCVD or UHVCVD.

31. The method of manufacturing a semiconductor device according to claim 30, wherein the LPCVD is applied by using a DCS-H<sub>2</sub>-HCl gas system or MS-H<sub>2</sub>-HCl gas system on the  
15 basis of a Si-H-Cl system.

32. The method of manufacturing a semiconductor device according to claim 31, wherein the DCS-H<sub>2</sub>-HCl gas system is applied, under the conditions that the temperature  
20 is between 750 and 850°C, the pressure is between 5 to 760 Torr, the flow rate of DCS is between 0.1 and 1slm, the flowrate of HCl is between 0.1 and 1.0slm, the flowrate of H<sub>2</sub> is between 30 and 150slm, and 1 and 10% PH<sub>3</sub>/H<sub>2</sub> is supplied at a flowrate of between 0.1 and 1.5 slm.

33. The method of manufacturing a semiconductor device according to claim 31, wherein the MS-H<sub>2</sub>-HCl gas system is applied, under the conditions that the temperature is between 750 and 850°C, the pressure is between 5 and 760 Torr, the flow rate of MS is 0.1 and 1slm, the flowrate of HCl is between 0.5 and 5.0 slm, the flowrate of H<sub>2</sub> is between 30 and 150slm, and 1 and 10% PH<sub>3</sub>/H<sub>2</sub> is supplied at a flowrate of between 0.1 and 1.5 slm.

34. The method of manufacturing a semiconductor device according to claim 27, further comprising the step of performing a wet cleaning process on the plasma-treated silicon substrate.

35. The method of manufacturing a semiconductor device according to claim 34, wherein the wet cleaning process comprises two steps, the first step performed, under the conditions that H<sub>2</sub>SO<sub>4</sub> and H<sub>2</sub>O<sub>2</sub> solutions are maintained at a ratio of between 1:1 and 100:1 and the temperature is between 80 and 120°C, for between 1 to 20 minutes, and the second step performed with a HF solution diluted in distilled water at a ratio of between 100:1 and 500:1 to remove oxide layers on the surface of silicon substrate.

36. The method of manufacturing a semiconductor device according to claim 27, wherein the contact hole is formed by a SAC method.

5 37. The method of manufacturing a semiconductor device according to claim 27, wherein the insulating layer is made of an oxide layer material including BPSG.

10 38. The method of manufacturing a semiconductor device according to claim 37, wherein the selective conductive plug is formed by using the difference of silicon growth speed in the nitride layer and in the oxide layer.

15 39. The method of manufacturing a semiconductor device according to claim 27, wherein the growth target of the selective conductive plug is between 60 to 100% of the width of the contact hole gap.

20 40. The method of manufacturing a semiconductor device according to claim 30, wherein the selective conductive plug is formed by UHVCVD using a  $\text{Si}_2\text{H}_6 + \text{Cl}_2 + \text{H}_2$  system, the flow rate of  $\text{Si}_2\text{H}_6$  is between 1 and 10sccm, the flowrate of  $\text{Cl}_2$  is up to 5sccm, the flowrate of  $\text{H}_2$  is up to 20sccm, and 1 to 10%  $\text{PH}_3/\text{H}_2$  is also supplied.

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41. The method of manufacturing a semiconductor device according to claim 40, wherein  $\text{GeH}_4$  is supplied at a flow rate of up to 10sccm.

5 42. The method of manufacturing a semiconductor device according to claim 30, wherein the UHVCVD method is performed in a UHVCVD device for a single wafer process and in a tube type UHVCVD for SEG.

10 43. The method of manufacturing a semiconductor device according to claim 27, wherein, prior to the step of forming the insulating layer, is a step further comprising forming a gate structure.

15 44. The method of manufacturing a semiconductor device according to claim 43, further comprising the step of forming a source and drain, before or after the selective conductive plug is formed.

20 45. The method of manufacturing a semiconductor device according to claim 44, wherein, if the source and drain are formed after the selective silicon plug is formed, a cell block mask is employed to protect the isolation layer on the cell region.

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46. The method of manufacturing a semiconductor device according to claim 45, wherein the cell block mask is separated from one end of the cell block by 1 to 10 $\mu$ m.

5 47. The method of manufacturing a semiconductor device according to claim 44, wherein, after the selective silicon plug is formed, the step of forming a source and drain comprises the steps of:

forming a sensitive film pattern by performing an  
10 exposure process;

forming an interlayer insulating layer on adjacent regions of the cell by using a wet etch process and removing the nitride layer spacer; and

performing an ion implantation process to form the  
15 source and drain.

48. The method of manufacturing a semiconductor device according to claim 47, further comprising the step of depositing an interlayer insulating layer and performing a  
20 planation process by CMP, after the source and drain are formed.